WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a bit line for transferring a signal changing between a first voltage and a second voltage higher than said first voltage;

a memory cell having an element for storing information and a selection gate for connecting said element to said bit line when selected, said selection gate being constituted of an insulated gate type field effect transistor;

a word line connected to the selection gate of said memory cell, for transferring a voltage determining selection and unselection of said element; and

word line voltage applying circuitry for applying said voltage to said word line, said word line voltage applying circuitry applying a third voltage outside a voltage changing range of said bit line when said element is unselected, and applying a fourth voltage when said element is selected, said third voltage being at a level for setting a reliability evaluation value of a gate insulating film of said selection gate to, at most, a reliability evaluation value of the gate insulating film when said fourth voltage is applied.

2. The semiconductor device according to claim 1, wherein

said third voltage is a negative voltage, and said first voltage is at a level of externally applied ground voltage.

3. The semiconductor device according to claim 1, wherein

said word line voltage applying circuitry includes a screening circuit for accelerating stress of the gate insulating film of said selection gate in an unselected state.

4. The semiconductor device according to claim 1, wherein

said word line voltage applying circuitry comprises a circuit for accelerating an electric field applied the gate insulating film of said

selection gate in a selected state, and a circuit for accelerating the electric field applied to the gate insulating film of said selection gage in an unselected state.

5. The semiconductor device according to claim 1, wherein said third voltage is at a level of externally applied ground voltage, and said first voltage is at a level higher than said third voltage.

6. The semiconductor device according to claim 1, wherein said third voltage is a voltage lower than said first voltage, and said fourth voltage is a voltage higher than said second voltage.

7. A semiconductor device comprising:

an internal circuitry having a power source node;

a power line transmitting a power source voltage;

a power supply control transistor formed of an insulated gate type field effect transistor, coupled between said power source node and said power line, set to a high impedance state when said internal circuitry is in an unselected state, and set to a low impedance state when said internal circuitry is in a selected state; and

control circuitry for applying a control signal to a gate of said power supply control transistor in response to an operation mode designation signal designating an operation mode of said internal circuitry, said control circuitry applying, as said control signal, a voltage for making a reliability evaluation value of a gate insulating film of said power supply control transistor in a high impedance state be not greater than a reliability evaluation value of the gate insulating film in said low impedance state..

8. The semiconductor device according to claim 7, wherein said control circuitry sets said control signal to a voltage level higher in absolute value than the power source voltage on said power line when said power supply control transistor is in a high impedance state.

9. The semiconductor device according to claim 7, wherein

said control circuitry includes a circuit for accelerating an electric field applied to a gate insulating film of said power supply control transistor when said power supply control transistor is in a high impedance state.

10. The semiconductor device according to claim 7, wherein

said power line transfers the power source voltage higher than a ground voltage, and said power supply control transistor is of a P channel type.

11. A semiconductor device comprising:

internal circuitry including a plurality of sub-circuits, said plurality of sub-circuits including a first sub-circuit connected to a first power line transferring a first power source voltage and a second sub-circuit connected to a second power line transferring a second power source voltage;

first power source circuitry connected to said first power line, for generating the first power source voltage, the first power source circuitry generating a second voltage larger in absolute value than a first voltage level generated in selection of said internal circuitry when said internal circuitry is unselected onto said power line as said first power source voltage; and

second power source circuitry connected to said second power line, for generating a voltage at the first voltage level as said second power source voltage independently of selection and unselection of said internal circuitry, a reliability evaluation value of a gate insulating film of a transistor of a sub-circuit of said internal circuitry in an unselected state being set, at most, to a reliability evaluation value of the gate insulating film of said internal circuit in a selected state.

12. The semiconductor device according to claim 11, wherein

said first power source circuitry includes a circuit for accelerating said first power source voltage generated when said internal circuitry is in

an unselected state.

13. The semiconductor device according to claim 11, wherein said second power source circuitry includes a circuit for accelerating said second power source voltage generated when said internal circuitry is in an unselected state.

14. The semiconductor device according to claim 11, further comprising:

a power source control transistor, formed of an insulated gate type transistor and connected between the first and second power lines, for electrically separating said first and second power lines when said internal circuitry is in an unselected state, a reliability evaluation value of a gate insulating film of said power source control transistor in the unselected state of the internal circuitry being set, at most, to a reliability evaluation value thereof in a selected state.

15. The semiconductor device according to claim 14, wherein said power source control transistor receives a voltage larger in absolute value said first power source voltage at a gate thereof for connecting said first and second power lines together when said internal circuitry is in the selected state.